## REMARKS

While it is believed that the previously pending claims satisfy the requirements of 35 USC §112, and also adequately distinguish the invention from the prior art, in order to expedite prosecution, Applicant has amended independent claim 37 to positively recite that the trench formed in the semiconductor substrate partitions the dummy area patterns from the active area patterns. Independent claim 41 has been amended to positively recite the step of forming a trench in the substrate to partition the dummy active areas from active areas using the first mask. No new matter has been entered.

Turning to the art rejections, and considering first the rejection of claims 37 and 39-41 under 35 USC § 103(a) as being obvious over Applicant's admitted prior art (APA) in view of Gilbert et al. (U.S. Patent No. 5,885,856), as the Examiner is no doubt aware, in order for a proper § 103 rejection to be formed, there must exist in the art some motivation to combine the references. In rejecting the claims as obvious from the APA in view of Gilbert et al., the Examiner acknowledges that the APA does not teach forming a first photoresist pattern layer, a first photoresist pattern layer. However, the Examiner takes the position that this missing teaching is provided by Gilbert et al. While Gilbert et al. may form isolation trenches to provide electrical isolation between various components of the integrated circuit (col. 2, lines 42-46), Gilbert et al. does not teach forming these trenches to partition dummy active areas from active area patterns, as required by independent claim 37 of the instant Application. In fact, Gilbert et al. teaches against the claimed invention in warning that the dummy structures must not intersect or come into contact with well boundaries (col. 3, lines 10-19), and proposes a method for

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determining which regions are active regions and which regions are dummy regions (col. 4, lines 19-51). Nowhere does Gilbert et al. teach or suggest using a first masking layer defining the active regions and dummy regions to form trenches, using that same masking layer to form trenches in the semiconductor substrate which partitions the dummy area patterns from the active area patterns, and using a second masking layer corresponding to the first masking layer to form active gates and dummy gates as required by Applicant's independent claim 37. Thus, Gilbert et al. cannot be combined with the Applicant's APA to render obvious claim 37 or claims 39-40 which depend thereon.

Similar comments apply to the rejection of claim 41, which, as noted *supra*, has been amended to positively recite the step of forming a trench in the substrate which partitions the dummy active areas from active areas by an etching process using the first mask. Thus, claim 41 also cannot be said to be obvious from the art.

Turning to the rejection of claim 38 as obvious from the APA in view of Gilbert et al. and further in view of the newly cited Patent to Shimomura et al. (U.S. Patent No. 6,140,687), claim 38 is dependent on claim 37. The deficiencies of the combination of the APA and Gilbert et al. vis-à-vis claim 37 are discussed above. It is not seen that Shimomura et al. supplies the missing teachings to the APA/Gilbert et al. combination to achieve or render obvious claim 37, or claim 38 which depends thereon. Shimomura et al. has been cited specifically to teach that it is conventional to form circular shaped gates. Even assuming *arguendo* the Examiner's characterization of Shimomura et al., the more basic and essential teachings missing from the APA/Gilbert et al. combination, as discussed above, are not supplied by Shimomura et al. Thus,

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no combination of the APA, Gilbert et al. and Shimomura et al. could achieve or render obvious claims 37 or 38 which depends thereon.

Having dealt with all the objections raised by the Examiner, it is believed that the Application now is in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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## **CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP - RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on Orbotal 21, 2003, at Tucson, Arizona.

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